REMARKS

The Applicant appreciates the thorough examination of the present application as evidenced by the Official Action mailed March 12, 2004 (hereinafter "the Official Action"). In particular, the Applicant appreciates the Examiner's indication that Claims 52-55 are allowed, and that Claims 2-9, 11-16, 18-23, 25-30, 32-37, 39-44, and 46-51 would be allowable if rewritten in independent form.

In response to the Official Action, the Applicant has amended Claims 1, 10, 17, 24, 31, 38, and 45 to more clearly define the claimed invention; and rewritten Claims 2, 11, 18, 25, 32, 39, and 46 in independent form. The Applicant will show in the following remarks that amended Claims 1, 10, 17, 24, 31, 38, and 45 are patentable over the cited art. Support for the amendments of Claims 1, 10, 17, 24, 31, 38, and 45 can be found, for example, in Figures 2C, 2D, and 2E and related portions of the specification.

Claims 2, 11, 18, 25, 32, 39, and 46 have been placed in a condition indicated allowable in the Official Action. In addition, the Applicant has amended Claims 17, 18, 20, 31, 32, 45, 46, 48, and 53 to correct minor typographical errors noted therein; and the Applicant has added new Dependent Claims 56-62 which are patentable for at least the reasons discuss below with regard Claims 1, 10, 17, 24, 31, 38, and 45.

Accordingly, the Applicant submits that all claims are in condition for allowance for at least the reasons discussed in greater detail below.

Independent Claims 1, 10, 17, 24, 31, 38, And 45 Are Patentable

Claims 1, 10, 17, 24, 31, 38, and 45 have been rejected "under 35 U.S.C. § 103(a) as being unpatentable over the article by Gordon L. Smith entitled "Model for delay faults based upon paths," 1985 International test conference, Paper 9.6, pages 342-349 (hereinafter "the Smith article"). Claims 1 and 10, however, are patentable for at least the reasons discussed below.

Claim 1, for example, recites a method for characterizing a fault in an integrated circuit device, the integrated circuit device comprising primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs. More particularly, the method includes:

> defining a fault tuple including an identification of a signal line, a signal line value, and a clock cycle constraint for the signal line such that the fault tuple is satisfied by providing a test sequence comprising one or more test patterns such that the signal line is controlled to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint responsive to application of the test sequence to the primary inputs wherein the signal line identified by the fault tuple is not directly coupled to any of the primary inputs and wherein the signal line is not directly coupled to any of the primary outputs.

In contrast to the recitations of Claim 1, the Smith article discusses a model for delay faults based upon paths (as opposed to fault tuples). As discussed in the Smith article:

> This is a global delay fault model because it is associated with an entire path. The more familiar slow-to-rise or slow-to-fall gate delay fault, on the other hand, is a local fault mode. A procedure is described which identifies paths which are tested for path faults by a set of patterns. It does not involve delay simulation. The paths so identified are tested for path faults independent of the delays of any individual gate of the network.

Smith, page 342, col. 1 (emphasis added). Moreover:

> This protocol is intended to detect delay faults within the combinational network which cause the propagation time of the network to exceed the clock interval. It is assumed, for purposes of this paper, that there are no other types of faults.

Smith, page 342, col. 1 (emphasis added). The Smith article further states that:

> A list of paths is provided. For purposes of the algorithm, each path is described as a transition direction and a list of gates from the output backwards to the input.

Smith, page 346, col. 1 (emphasis added).

As discussed above, the Smith article defines a path as opposed to defining a fault tuple including an identification of a signal line (not directly coupled to any primary inputs or to any primary outputs), a signal line value, and a clock cycle constraint for the signal line value. The Smith article thus teaches away from defining a fault tuple including an identification of a signal line (not directly coupled to any primary inputs or to any primary outputs), a signal line value, and a clock cycle constraint for the signal line. The Smith article also fails to teach or suggest that a fault tuple is satisfied by providing a test sequence comprising one or more test patterns such that the signal line (not directly coupled to any primary inputs or to any

primary outputs) is controlled to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint responsive to application of the test sequence to the primary inputs.

The Official Action takes the position that, "It would have been obvious ... to realize that he [Smith] teaches a signal line that is controlled to the signal line value during a clock cycle of the test sequence, since he teaches a clock that samples the output of the network into another set of latches is timed to occur at the same time interval as the previous clock." Official Action, pages 2-3. As discussed above, however, the Smith article discusses a global delay fault model associated with an entire path wherein an identified path is tested for path faults independent of delays of any individual gate of the network. Accordingly, the Applicant respectfully submits that Smith teaches away from defining a fault tuple including an identification of a signal line (not directly coupled to any primary inputs or to any primary outputs), a signal line value, and a clock cycle constraint from the signal line such that the fault tuple is satisfied by providing a test sequence.

The Applicant thus respectfully submits that the Smith article fails to teach or suggest the method of Claim 1 and that Claim 1 is patentable over the Smith article. The Applicant further submits that Claims 10, 17, 24, 31, 38, and 45 are patentable over the Smith article for reasons similar to those discussed above with regard to Claim 1. If the Examiner should maintain any rejections based on the Smith article, the Applicant respectfully requests that the Examiner point out specific portions of the Smith article that teach defining a fault tuple including an identification of a signal line not directly coupled to any primary inputs or to any primary outputs, a signal line value, and a clock cycle constraint for the signal line such that the fault tuple is satisfied by providing a test sequence.

CONCLUSION

Accordingly, the Applicant submits that all pending claims in the present application are in condition for allowance, and allowance of all claims is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any additional issues should need to be addressed.

Respectfully submitted,

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